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- ☐ 1. **Dynamic clock management for low power applications in FPGAs**
Brynjolfson, I.; Zilic, Z.;
Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000
21-24 May 2000 Page(s):139 - 142
Digital Object Identifier 10.1109/CICC.2000.852635
[AbstractPlus](#) | [Full Text: PDF\(344 KB\)](#) IEEE CNF
- ☐ 2. **Asynchronous processor survey**
Werner, T.; Akella, V.;
Computer
Volume 30, Issue 11, Nov. 1997 Page(s):67 - 76
Digital Object Identifier 10.1109/2.634866
[AbstractPlus](#) | [References](#) | [Full Text: PDF\(352 KB\)](#) IEEE JNL
- ☐ 3. **Router plugins: a software architecture for next-generation routers**
Decasper, D.; Dittia, Z.; Parulkar, G.; Plattner, B.;
Networking, IEEE/ACM Transactions on
Volume 8, Issue 1, Feb. 2000 Page(s):2 - 15
Digital Object Identifier 10.1109/90.836474
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- ☐ **1. RNS-based enhancements for direct digital frequency synthesis**
Chren, W.A.;
Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on [see also Circuits and Systems II: Express Briefs, IEEE Transactions on]
Volume 42, Issue 8, Aug. 1995 Page(s):516 - 524
Digital Object Identifier 10.1109/82.404073
[AbstractPlus](#) | Full Text: [PDF\(712 KB\)](#) IEEE JNL
- ☐ **2. Circuit techniques in a 266-MHz MMX-enabled processor**
Draper, D.; Crowley, M.; Holst, J.; Favor, G.; Schoy, A.; Trull, J.; Ben-Meir, A.; Khanna, R.; Wendell, D.; Krishna, R.; Nolan, J.; Mallick, D.; Partovi, H.; Roberts, M.; Johnson, M.; Lee, T.;
Solid-State Circuits, IEEE Journal of
Volume 32, Issue 11, Nov. 1997 Page(s):1650 - 1664
Digital Object Identifier 10.1109/4.641685
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(328 KB\)](#) IEEE JNL
- ☐ **3. Design of a configurable accelerator for moment computation**
Hung, D.L.; Cheng, H.D.; Sengkhomyong, S.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 8, Issue 6, Dec. 2000 Page(s):741 - 746
Digital Object Identifier 10.1109/92.902269
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(228 KB\)](#) IEEE JNL
- ☐ **4. Itsy: stretching the bounds of mobile computing**
Hamburgen, W.R.; Wallach, D.A.; Viredaz, M.A.; Brakmo, L.S.; Waldspurger, C.A.; Bartlett, J.F.; Mann, T.; Farkas, K.I.;
Computer
Volume 34, Issue 4, April 2001 Page(s):28 - 36
Digital Object Identifier 10.1109/2.917534
[AbstractPlus](#) | [References](#) | Full Text: [PDF\(1756 KB\)](#) IEEE JNL



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- ☐ 1. **The Transmogriifier-2: a 1 million gate rapid-prototyping system**
Lewis, D.M.; Galloway, D.R.; Van Ierssel, M.; Rose, J.; Chow, P.; Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 6, Issue 2, June 1998 Page(s):188 - 198
Digital Object Identifier 10.1109/92.678867
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(192 KB) IEEE JNL
- ☐ 2. **IP validation for FPGAs using Hardware Object Technology™**
Casselmann, S.; Schewel, J.; Beaumont, C.; Parallel and Distributed Processing, 1999. 13th International and 10th Symposium on Parallel and Distributed Processing, 1999. 1999 IPSP/SPDP. Proceedings 12-16 April 1999 Page(s):624 - 629
Digital Object Identifier 10.1109/IPSP.1999.760542
[AbstractPlus](#) | Full Text: [PDF](#)(136 KB) IEEE CNF
- ☐ 3. **RIFLE-62: a flexible environment for prototyping dynamically reconfigurable systems**
Vasilko, M.; Long, D.; Rapid System Prototyping, 1998. Proceedings. 1998 Ninth International Workshop on 3-5 June 1998 Page(s):130 - 135
Digital Object Identifier 10.1109/IWRSP.1998.676681
[AbstractPlus](#) | Full Text: [PDF](#)(92 KB) IEEE CNF
- ☐ 4. **A new synthesis efficient, high density and high speed ORCA FPGA**
Singh, S.; Britton, B.; Spivak, C.; Nguyen, H.; Leung, W.-B.; Andrews, B.; Powell, G.; Albu, R.; He, J.; Stuby, R.; Chin, M.-L.; Chiu, P.-L.; Steward, J.; Rabold, D.; Custom Integrated Circuits Conference, 1997., Proceedings of the IEEE 1997 5-8 May 1997 Page(s):543 - 546
Digital Object Identifier 10.1109/CICC.1997.606685
[AbstractPlus](#) | Full Text: [PDF](#)(356 KB) IEEE CNF
- ☐ 5. **Hardware/software codesign and rapid prototyping of embedded systems**
Slomka, F.; Dorfel, M.; Munzenberger, R.; Hofmann, R.; Design & Test of Computers, IEEE Volume 17, Issue 2, April-June 2000 Page(s):28 - 38
Digital Object Identifier 10.1109/54.844331
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(140 KB) IEEE JNL
- ☐ 6. **Real time image integrator for magnetic surface mapping experiments in TJ-I U torsatron**
Marin, J.; Carballo, I.; Olmos, P.; Ascasibar, E.; Pastor, I.; Qin, J.; Herranz, J.; Fraguas, A.L.; Nuclear Science, IEEE Transactions on Volume 43, Issue 1, Part 1, Feb. 1996 Page(s):234
Digital Object Identifier 10.1109/23.486038
[AbstractPlus](#) | Full Text: [PDF](#)(288 KB) IEEE JNL
7. **Seeking solutions in configurable computing**

- ☐ Mangione-Smith, W.H.; Hutchings, B.; Andrews, D.; DeHon, A.; Ebeling, C.; Hartenstein, R.; Mencer, O.; Morris, J.; Palem, K.; Prasanna, V.K.; Spaanenburg, H.A.E.;
Computer
Volume 30, Issue 12, Dec. 1997 Page(s):38 - 43
Digital Object Identifier 10.1109/2.642810
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(80 KB) IEEE JNL
- ☐ **8. The flexibility of configurable computing**
Villasenor, J.; Hutchings, B.;
Signal Processing Magazine, IEEE
Volume 15, Issue 5, Sept. 1998 Page(s):67 - 84
Digital Object Identifier 10.1109/79.708541
[AbstractPlus](#) | Full Text: [PDF](#)(5100 KB) IEEE JNL
- ☐ **9. ANT-on-YARDS: FPGA/MPU hybrid architecture for telecommunication data processing**
Tsutsui, A.; Miyazaki, T.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 6, Issue 2, June 1998 Page(s):199 - 211
Digital Object Identifier 10.1109/92.678868
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(332 KB) IEEE JNL
- ☐ **10. An implementation of fuzzy logic controller on the reconfigurable FPGA system**
Daijin Kim;
Industrial Electronics, IEEE Transactions on
Volume 47, Issue 3, June 2000 Page(s):703 - 715
Digital Object Identifier 10.1109/41.847911
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(560 KB) IEEE JNL
- ☐ **11. BIST-based test and diagnosis of FPGA logic blocks**
Abramovici, M.; Stroud, C.E.;
Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
Volume 9, Issue 1, Feb. 2001 Page(s):159 - 172
Digital Object Identifier 10.1109/92.920830
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(232 KB) IEEE JNL
- ☐ **12. Error-driven edge selection for $\Sigma\Delta$ modulated signals to suppress in-band noise due to non-uniform sampling**
Eel-Wan Lee; Soo-Ik Chae;
Electronics Letters
Volume 34, Issue 7, 2 April 1998 Page(s):618 - 619
[AbstractPlus](#) | Full Text: [PDF](#)(240 KB) IEE JNL
- ☐ **13. A matrix converter induction motor drive using intelligent gate drive level current commutation techniques**
Empringham, L.; Wheeler, P.; Clare, J.;
Industry Applications Conference, 2000. Conference Record of the 2000 IEEE
Volume 3, 8-12 Oct. 2000 Page(s):1936 - 1941 vol.3
Digital Object Identifier 10.1109/IAS.2000.882143
[AbstractPlus](#) | Full Text: [PDF](#)(524 KB) IEEE CNF
- ☐ **14. Evolvable platform for array processing: a one-chip approach**
Girau, B.; Marchal, P.; Nussbaum, P.; Tisserand, A.; Restrepo, H.F.;
Microelectronics for Neural, Fuzzy and Bio-Inspired Systems, 1999. MicroNeuro '99.
Proceedings of the Seventh International Conference on
7-9 April 1999 Page(s):187 - 193
Digital Object Identifier 10.1109/MN.1999.758863
[AbstractPlus](#) | Full Text: [PDF](#)(84 KB) IEEE CNF
- ☐ **15. Approaching evolvable hardware to reality: The role of dynamic reconfiguration and virtual meso-structures**
Moreno, J.M.; Cabestany, J.; Madrenas, J.; Canto, E.; Faura, J.; Insenser, J.M.;
Microelectronics for Neural, Fuzzy and Bio-Inspired Systems, 1999. MicroNeuro '99.
Proceedings of the Seventh International Conference on
7-9 April 1999 Page(s):163 - 170
Digital Object Identifier 10.1109/MN.1999.758860
[AbstractPlus](#) | Full Text: [PDF](#)(236 KB) IEEE CNF

- ☐ **16. Table of Contents**
Circuits and Systems, 1998. Proceedings. 1998 Midwest Symposium on
9-12 Aug. 1998 Page(s):v - xv
[AbstractPlus](#) | Full Text: [PDF\(472 KB\)](#) IEEE CNF
- ☐ **17. Stimulus generation for built-in self-test of charge-pump phase-locked loops**
Veillette, B.R.; Roberts, G.W.;
Test Conference, 1998. Proceedings. International
18-23 Oct. 1998 Page(s):698 - 707
Digital Object Identifier 10.1109/TEST.1998.743214
[AbstractPlus](#) | Full Text: [PDF\(732 KB\)](#) IEEE CNF
- ☐ **18. Run-time monitoring of communication activities in a rapid prototyping environment**
Kirschbaum, A.; Becker, J.; Glesner, M.;
Rapid System Prototyping, 1998. Proceedings. 1998 Ninth International Workshop on
3-5 June 1998 Page(s):52 - 57
Digital Object Identifier 10.1109/IWRSP.1998.676668
[AbstractPlus](#) | Full Text: [PDF\(80 KB\)](#) IEEE CNF
- ☐ **19. Automating qualification of reconfigurable cores**
Luk, W.; Siganos, D.; Fowler, T.;
Reconfigurable Systems (Ref. No. 1999/061), IEE Colloquium on
10 March 1999 Page(s):4/1 - 4/6
[AbstractPlus](#) | Full Text: [PDF\(436 KB\)](#) IEE CNF
- ☐ **20. A 3-D re-configurable image processing element**
O'Donnell, L.; Williams, G.L.; Lacey, A.J.; Seed, N.L.; Thorne, P.R.; Zawada, A.C.; Ivey, P.A.;
High Performance Architectures for Real-Time Image Processing (Ref. No. 1998/197), IEE
Colloquium on
12 Feb. 1998 Page(s):1/1 - 1/7
[AbstractPlus](#) | Full Text: [PDF\(484 KB\)](#) IEE CNF

